

FIG. 1 (PRIOR ART)

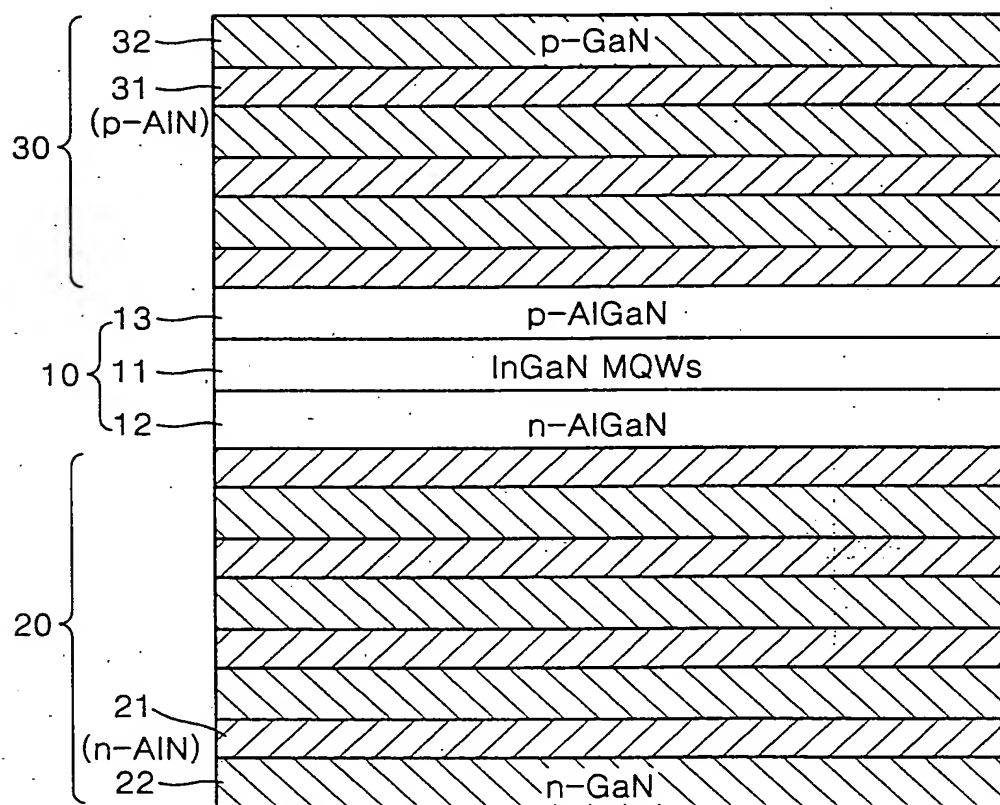


FIG. 2

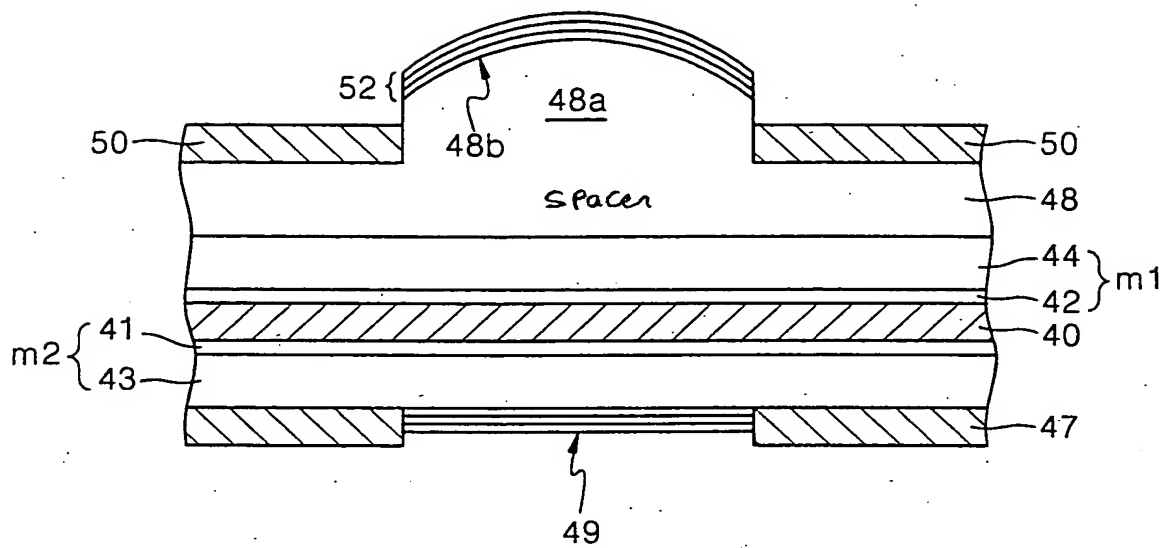


FIG. 3

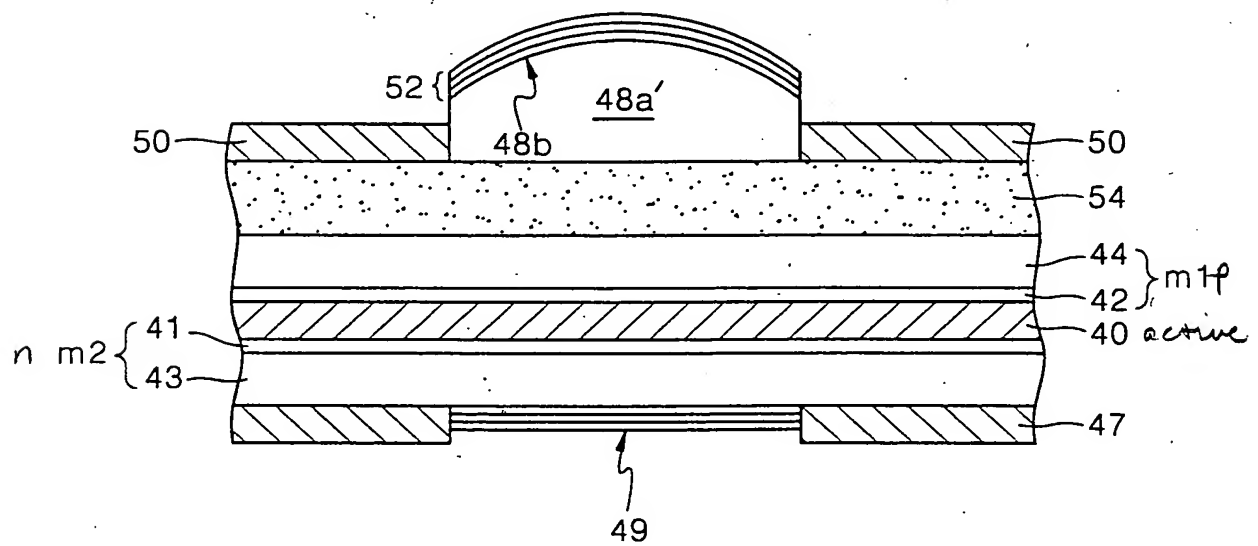


FIG. 4

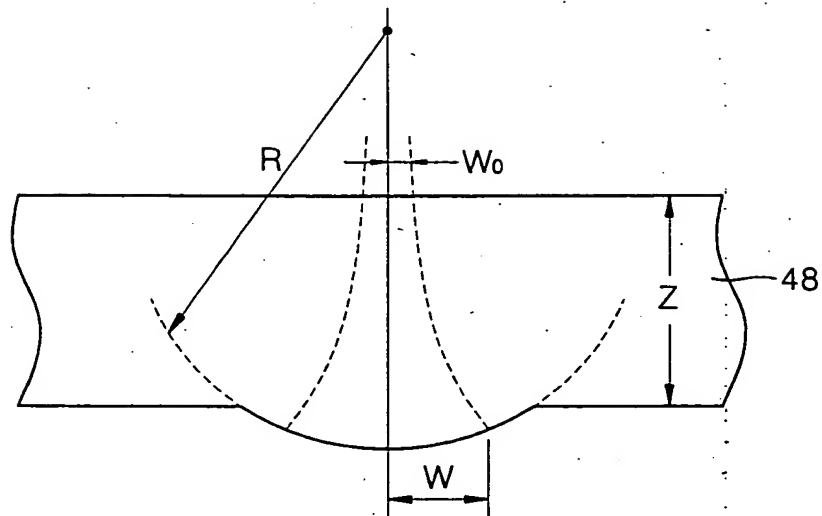


FIG. 5

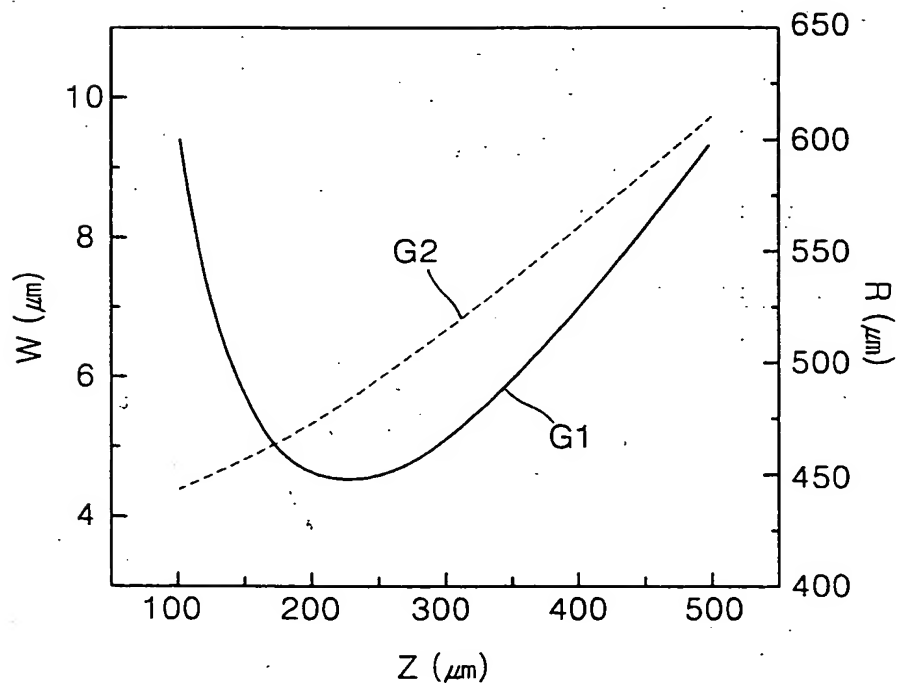


FIG. 6

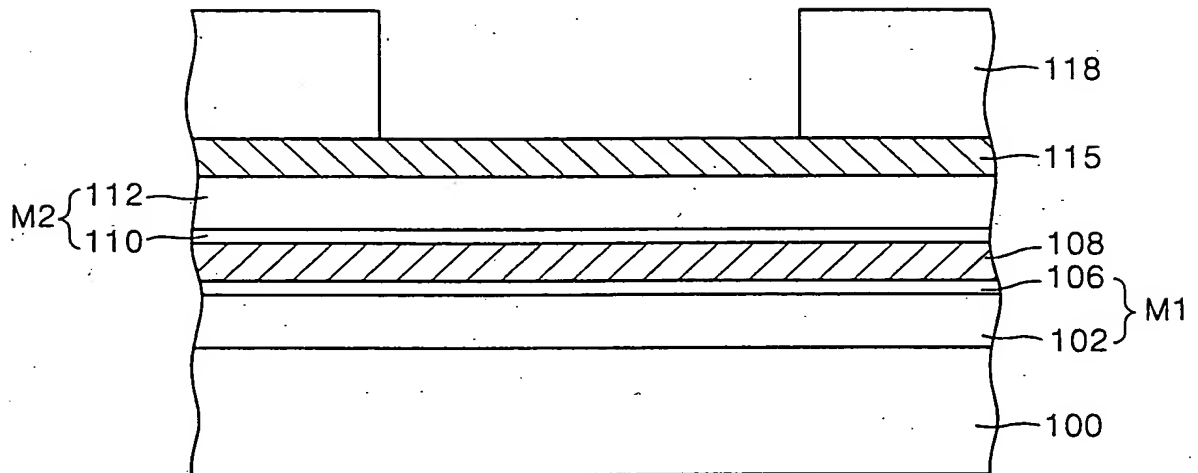


FIG. 7

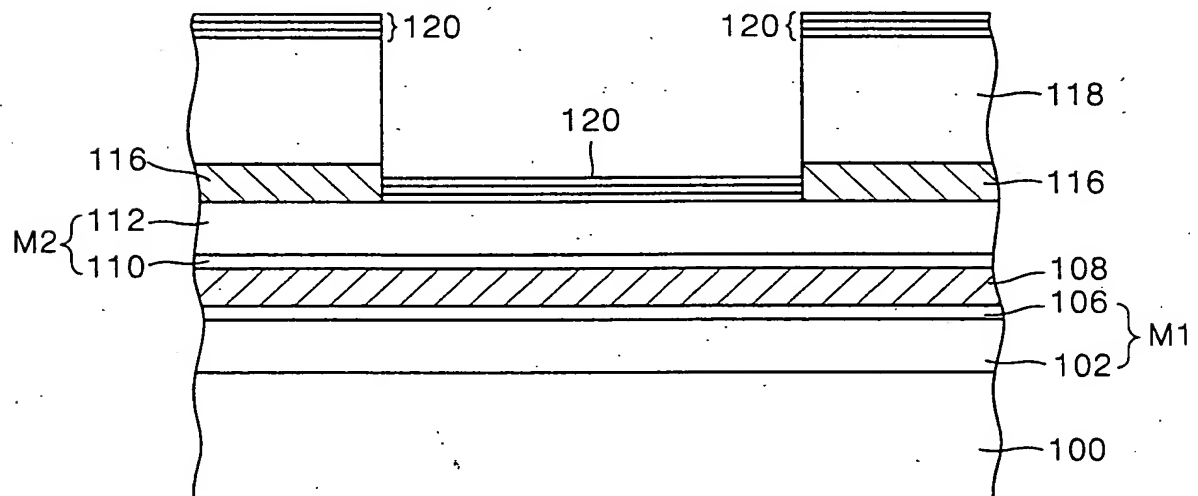


FIG. 8

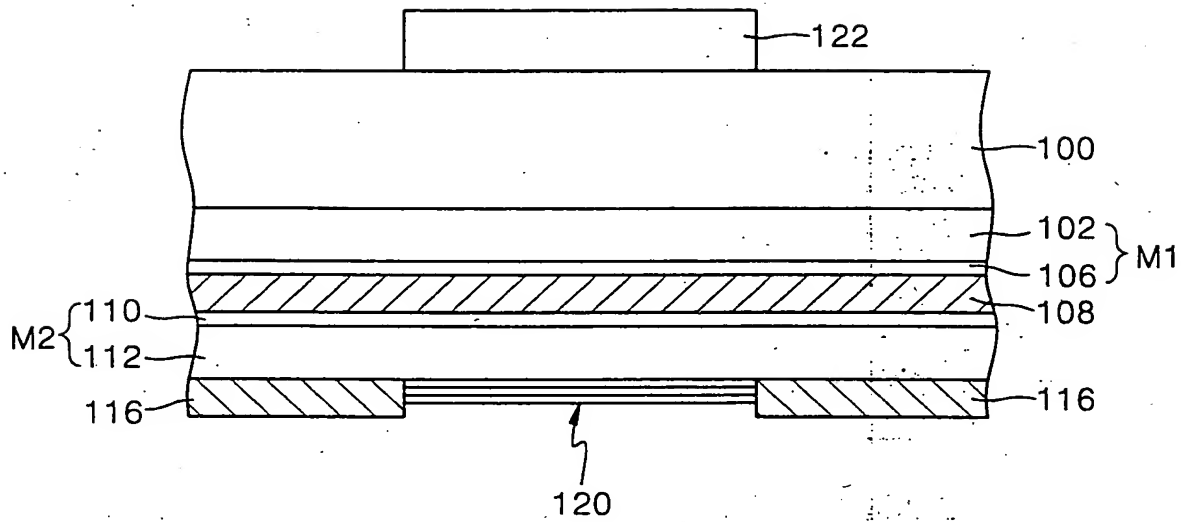


FIG. 9

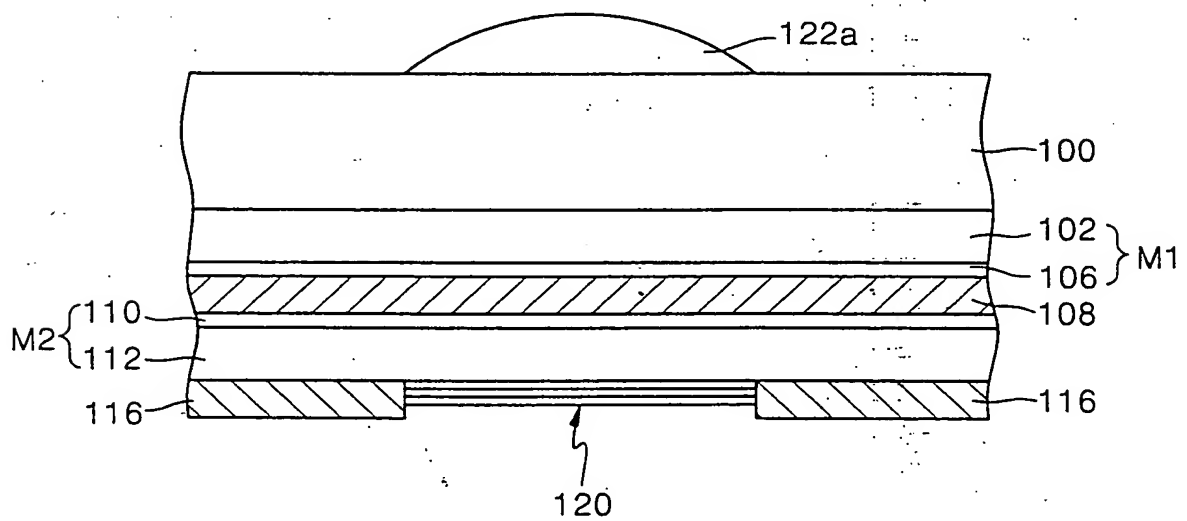


FIG. 10

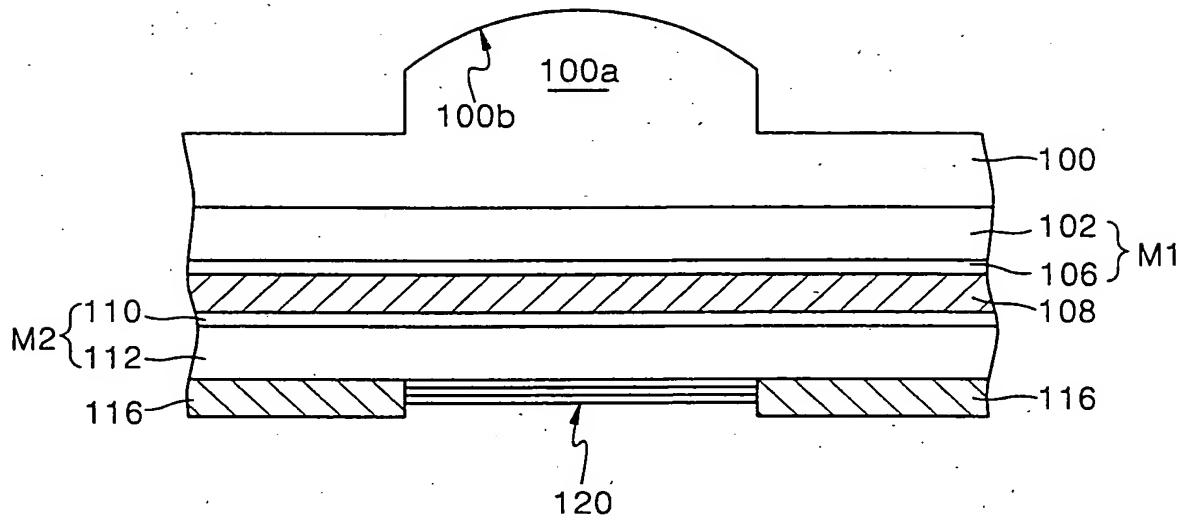
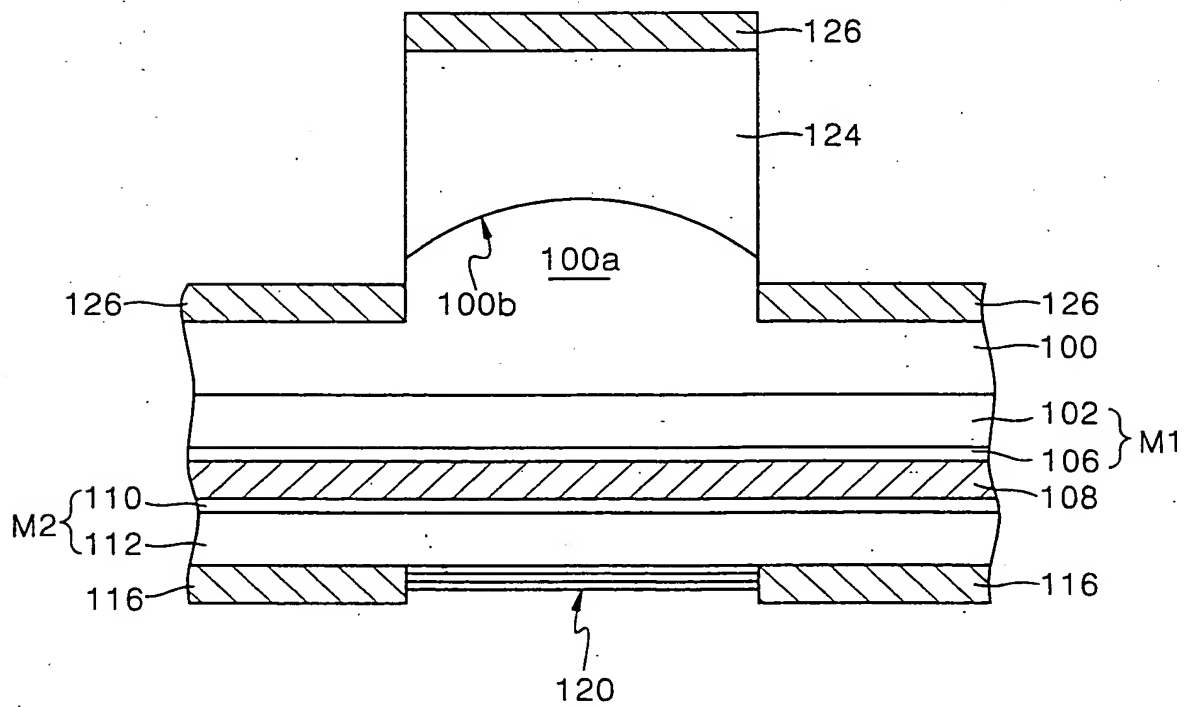


FIG. 11



A cross-sectional view of a semiconductor device 100a. The device features a central raised region 130 with a curved top surface 100b. The base of the device is composed of several layers: a bottom layer 116, a layer 112, a layer 110, a layer 108, a layer 106, and a top layer 102. These layers are grouped into two main sections: M1 (layers 102, 106, 108) and M2 (layers 110, 112). The device is flanked by side regions 126. A central channel or gap 120 is located beneath the raised region 130.

FIG. 14

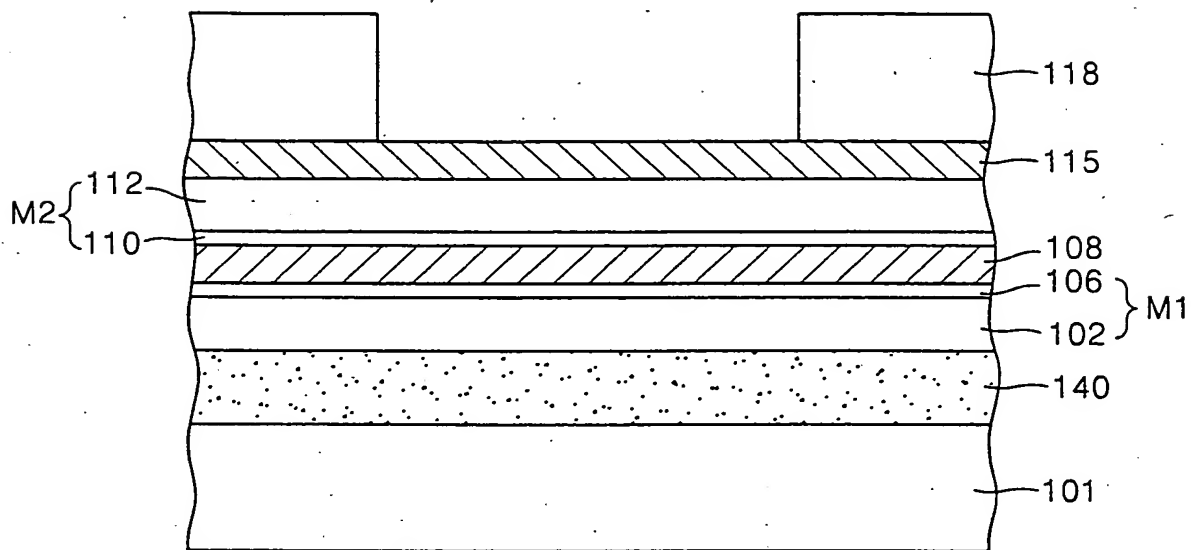


FIG. 15

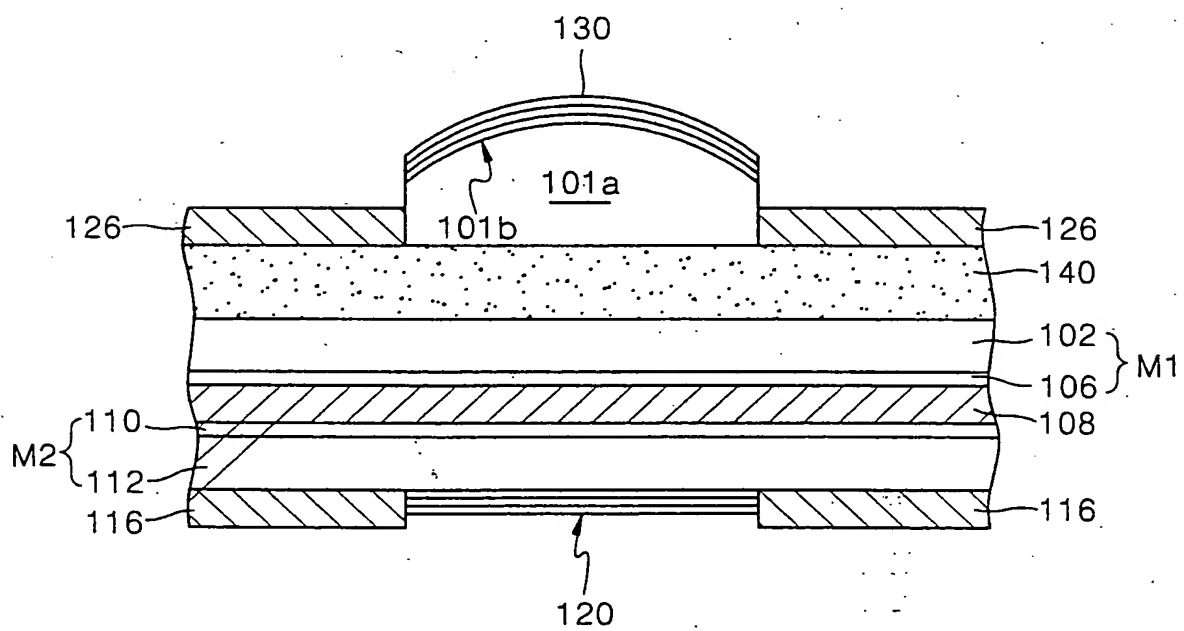




FIG. 16

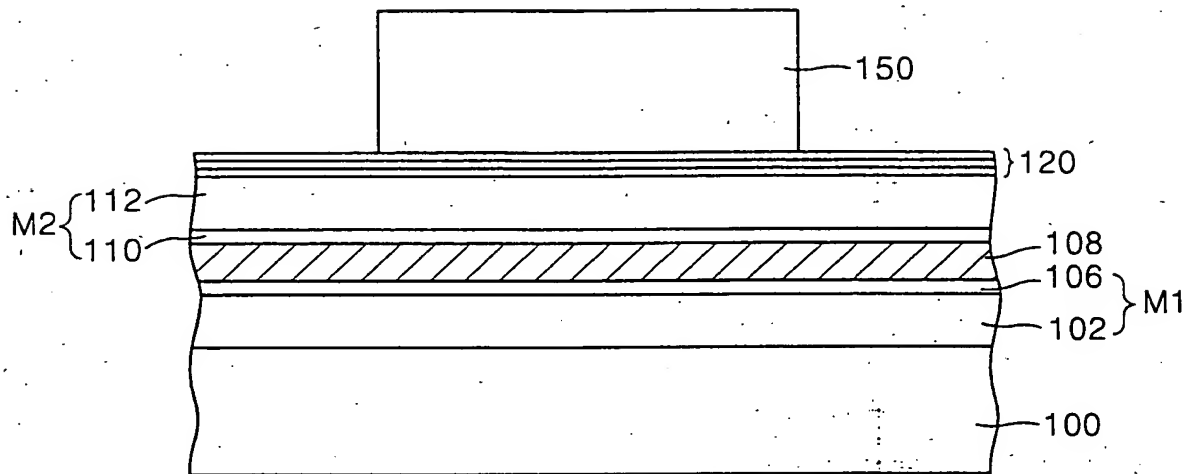


FIG. 17

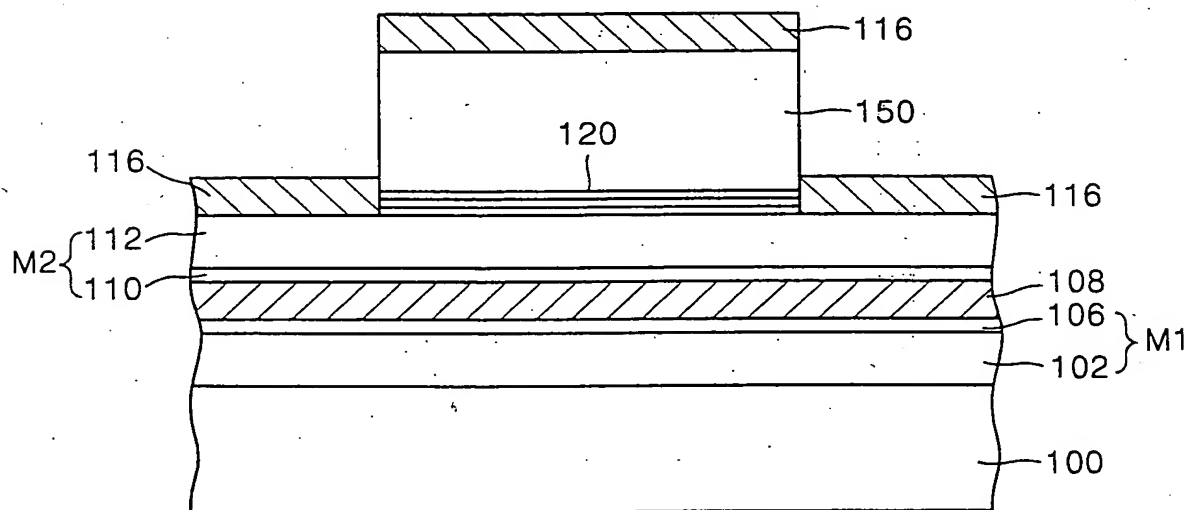


FIG. 18

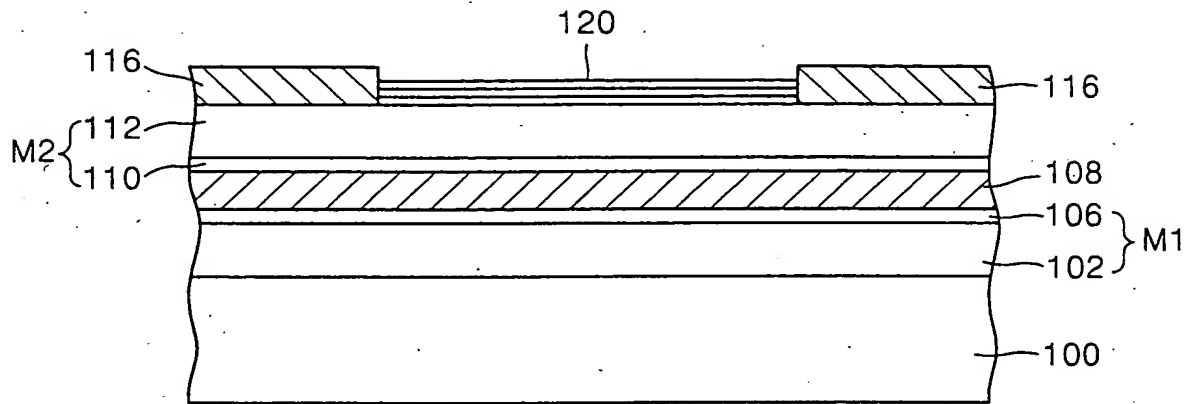


FIG. 19

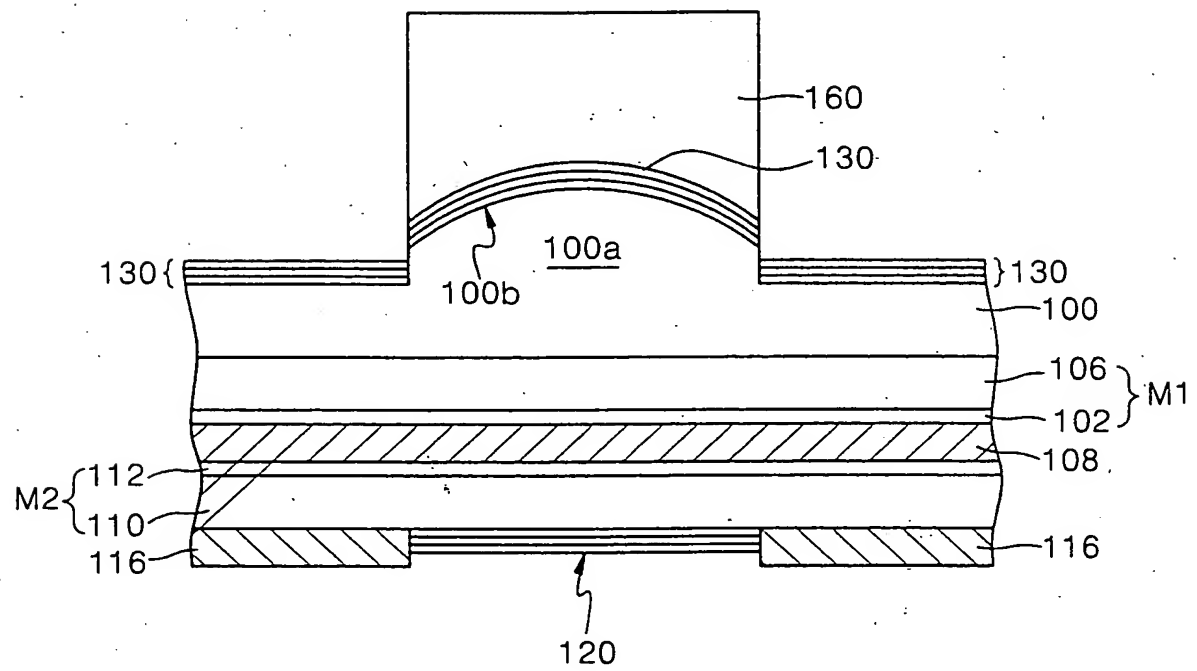


FIG. 20

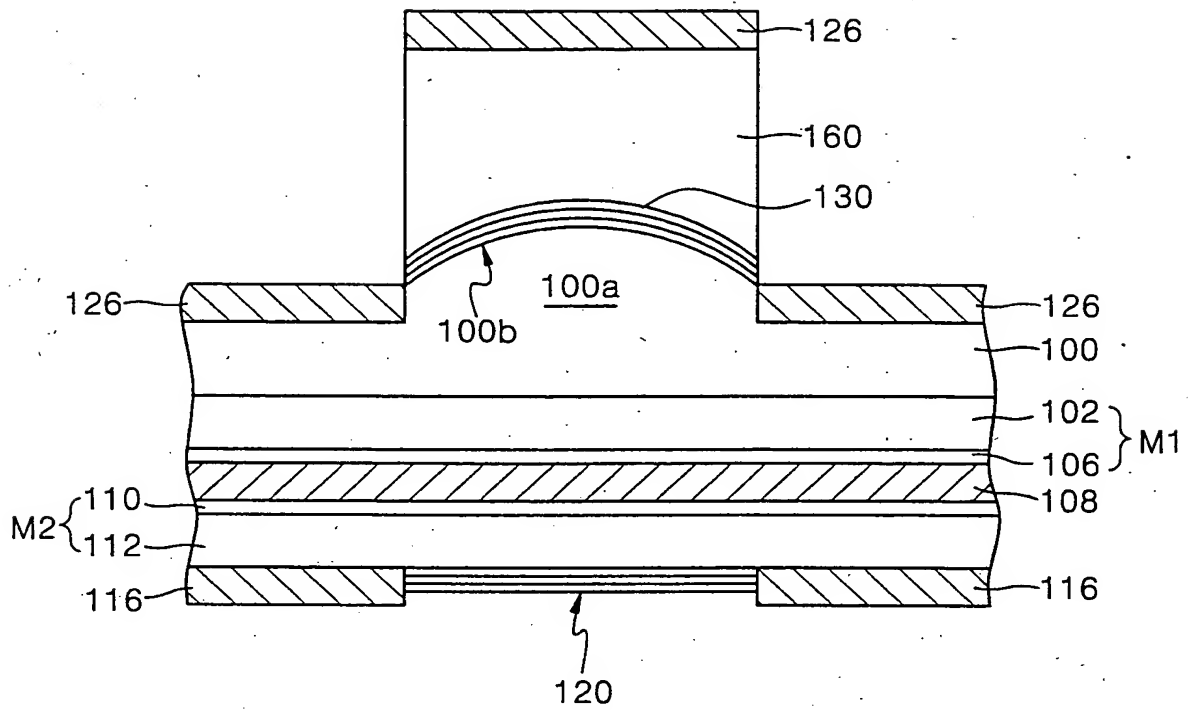


FIG. 21

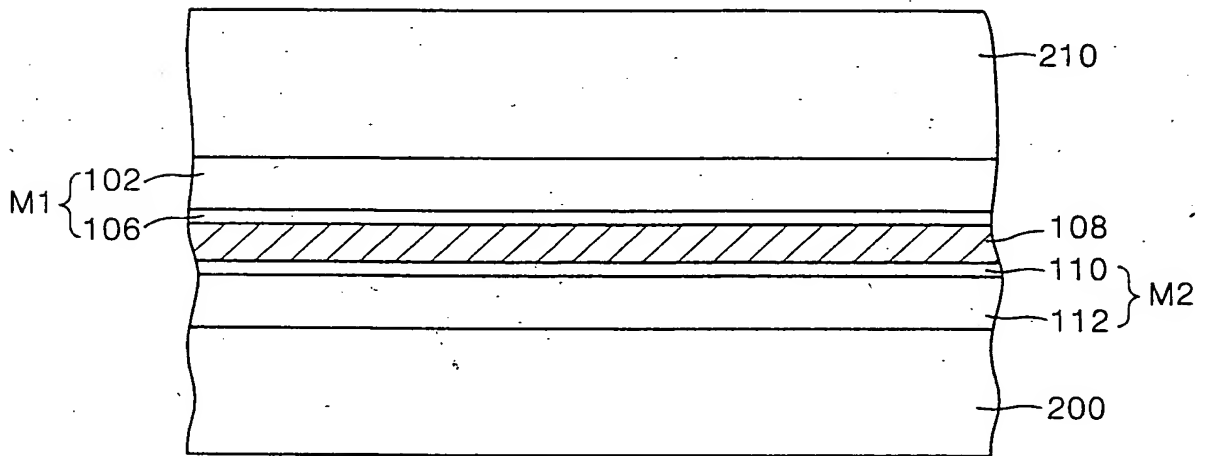


FIG. 22

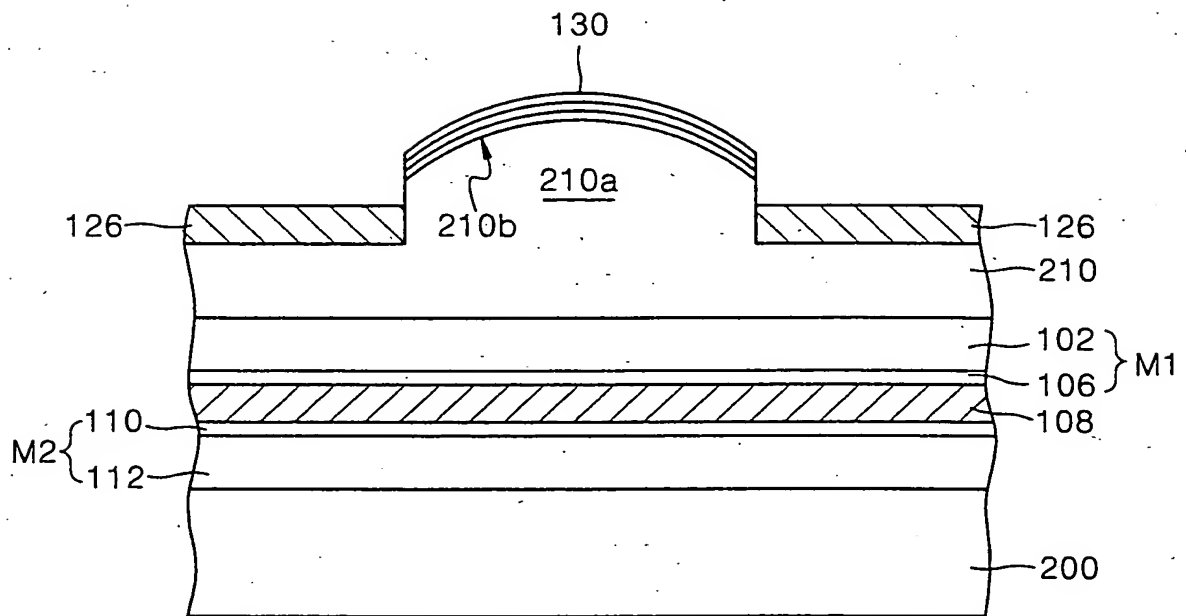


FIG. 23

